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EXAMINER
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PROCTOR, JASON SCOTT

ART UNIT	PAPER NUMBER
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2123

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	02/16/2007	PAPER

**Please find below and/or attached an Office communication concerning this application or proceeding.**

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

# Office Action Summary

Application No.

10/698,805

Applicant(s)

SZPAK ET AL.

Examiner

Jason Proctor

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

## Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☒ Responsive to communication(s) filed on 15 December 2006.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 1-10,32-37 and 42 is/are pending in the application.
- 4a) Of the above claim(s) 11-31,38-41,43 and 44 is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-10,32-37 and 42 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☒ Claim(s) 11-31,38-41,43 and 44 are subject to restriction and/or election requirement.

## Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 31 October 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

## Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
  - ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

## Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO/SB/08)  
Paper No(s)/Mail Date 4/11/05, 1/9/06.

- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_.
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: \_\_\_\_\_.

### **DETAILED ACTION**

Claims 11-31, 38-41, and 43-44 are withdrawn as a result of the election set forth below.

Claims 1-10, 32-37, and 42 are pending in this application.

Claims 1-10, 32-37, and 42 are rejected.

#### ***Restriction Requirement***

1. Applicant's election without traverse of Invention I (claims 1-10, 32-37, and 42) in the reply filed on 15 December 2006 is acknowledged.

Applicant is reminded that upon the cancellation of claims to a non-elected invention, the inventorship must be amended in compliance with 37 CFR 1.48(b) if one or more of the currently named inventors is no longer an inventor of at least one claim remaining in the application. Any amendment of inventorship must be accompanied by a request under 37 CFR 1.48(b) and by the fee required under 37 CFR 1.17(i).

#### ***Claim Rejections - 35 USC § 101***

2. Claims 1-10 are rejected under 35 U.S.C. § 101 because the claimed invention is directed to non-statutory subject matter.

Claim 1 defines a method consisting of two steps: "grouping [two signals]" and "performing [an operation]". A broad, reasonable interpretation of these steps encompasses an abstract or mental "grouping," and "performing" an abstract or mental operation on the grouped

signals. Such a method of abstract or mental steps falls under the 35 U.S.C. § 101 Judicial Exception of Abstract Ideas (MPEP 2106(IV)(C)). To be patent-eligible subject matter, the method must be limited to a practical application (MPEP 2106(IV)(C)(2)) by (A) “transforming” an article or physical object to a different state or thing; or (B) otherwise producing a useful, concrete, and tangible result.

The claimed invention does not “transform” an article or physical object to a different state or thing because the claim language is broad enough to encompass all manner of “non-virtual operations” performed on a “bus signal in a graphical model displayed on a graphical user interface.” These “non-virtual operations” may modify properties of the abstract bus signal “displayed on a graphical user interface,” but doing so does not “transform” an article or physical object to a different state or thing.

The claimed invention does not produce a useful, concrete, and tangible result. In particular, the invention is not limited to producing a tangible result. The scope of the term “non-virtual operation” is broad enough to encompass, for example, modifying intangible properties of the abstract bus signal “displayed on a graphical user interface.”

Therefore, the claimed method does not (A) “transform” an article or physical object to a different state or thing; or (B) otherwise producing a useful, concrete, and tangible result. The method is directed to nonstatutory subject matter.

To overcome this rejection, the Examiner respectfully suggests incorporating language that specifies a *tangible* result for the method, such as the language of claim 2 which defines the construction of a particular block diagram display.

Claims rejected but not specifically mentioned stand rejected by virtue of their dependence.

To expedite a complete examination of the instant application the claims rejected under 35 U.S.C. § 101 (nonstatutory) above are further rejected as set forth below in anticipation of applicant amending these claims to place them within the four statutory categories of invention.

### ***Claim Rejections - 35 USC § 112***

The following is a quotation of the second paragraph of 35 U.S.C. § 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 1-10, 32-37, and 42 are rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 1, 32, and 42 recite “performing a *non-virtual operation* on the bus signal” (or similar language) which renders the claim vague and indefinite. It is presumed that Applicants’ act as their own lexicographer and that the phrase *non-virtual operation* refers to a special definition as this term is not well known in the art. However, neither the disclosure nor the claims set forth an explicit and deliberate definition for this term.

The specification describes “virtual” and “nonvirtual” blocks, but does not explicitly define non-virtual operations [*“In Simulink® and other graphical modeling environments, the nodes, blocks or other model components used to model a dynamic system are generally either ‘virtual’, meaning the blocks play no active role in a simulation or ‘nonvirtual’, meaning the blocks play an active role in simulating a system represented by the graphical model.”* (page 3,

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third paragraph)]. The specification describes simulating an operation, but does not provide an explicit and deliberate definition for the term [*"To simulate an operation on signals in a bus signal having different data types, the signals must be de-grouped prior to passing each signal separately through a non-virtual block representing an operation to be performed on the signal."* (page 4, second paragraph)].

The specification provides a description of the operations performed by a "non-virtual block," however this description is exemplary in nature and does not specifically define what should be regarded as a virtual or non-virtual operation [*"The non-virtual block 407 represents an operation to be performed on the signal values represented by all of the signals 42, 44 and 46 within the bus signal 410, to simulate a non-virtual operation on all of the signals contained within the bus signal 410 without requiring a separate operation block for each component signal. Examples of non-virtual operations include, but are not limited to multiplication using a 'Gain' block, integration using an 'Integrator' block, calculating a derivative of an input using a 'Derivative' block, delaying an input using a 'Delay' block, and many others known in the art or created by the user."* (page 14, first paragraph)]. The language, "and many others known in the art or created by the user" contributes to the indefiniteness of the claim language.

Therefore, the metes and bounds of the claimed invention are indefinite because the precise definition of a "non-virtual operation" is unknown.

Claims rejected but not specifically mentioned stand rejected by virtue of their dependence.

***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. § 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1, 32, and 42 are rejected under 35 U.S.C. § 102(e) as being anticipated by US Patent No. 7,167,817 to Mosterman et al. (Mosterman).

The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention “by another,” or by an appropriate showing under 37 CFR 1.131.

Regarding claims 1, 32, and 42, Mosterman discloses a system, medium, and method for generating and displaying a modeling application for simulating a dynamic system, comprising:

a user-operable input means for inputting data into an application (FIG. 17, ref. 313);

a display device for displaying a graphical model representing the dynamic system (FIG. 17, ref 312); and

an electronic device including memory for storing computer program instructions and data (FIG. 17, ref 315 and 316), and a processor for executing the stored computer program

instructions (FIG. 17, ref 311), the computer program instructions including instructions for performing a non-virtual operation on a bus signal displayed in the graphical model, wherein the bus signal comprises first data signal of a first signal type and a second data signal of a second signal type grouped to form the bus signal [*"A virtual block is provided for graphical organizational convenience and plays no role in the definition of the system of equations described by the block diagram model. Examples of virtual blocks are the Bus Creator virtual block and Bus Selector virtual block which are used to reduce block diagram clutter by managing groups of signals as a "bundle".*" (column 5, lines 10-27)].

5. Claims 1, 2, 6, 7, 10, 32, 36, 37, and 42 are rejected under 35 U.S.C. 102(b) as being anticipated by US Patent No. 6,411,923 to Stewart et al. (Stewart).

Regarding claims 1, 2, 6, 7, 10 32, 33, 36, 37, and 42, Stewart discloses a system, medium, and method for generating and displaying a modeling application for simulating a dynamic system, comprising:

a user-operable input means for inputting data into an application (column 9, lines 10-26);

a display device for displaying a graphical model representing the dynamic system (column 9, lines 10-26); (FIG. 1, ref 136) and

an electronic device including memory for storing computer program instructions and data (FIG. 1, ref 132); (column 4, lines 10-33), and a processor for executing the stored computer program instructions (FIG. 1, ref 134); (column 4, lines 10-33), the computer program



instructions including instructions for performing a non-virtual operation on a bus signal displayed in the graphical model, wherein the bus signal comprises first data signal of a first signal type and a second data signal of a second signal type grouped to form the bus signal [ "*The Fieldbus protocol is an all digital, two-wire loop protocol.*" (column 2, lines 17-19); (FIG. 6A, 6B, etc.) showing bus segments connecting various "non-virtual" operational blocks, see (column 3, lines 28-42); (column 4, lines 10-33); (column 6, lines 40-67); etc.].

Regarding claims 2 and 33, Stewart discloses that the graphical model is a block diagram and the step of performing a non-virtual operation on the bus signal comprises constructing the block diagram including an operation block representing the non-virtual operation and connecting a representation of the bus signal in the block diagram to an input port of the operation block (FIG. 6A, 6B, etc.).

Regarding claims 6 and 36, Stewart discloses defining one or more physical attributes for the first data signal and the second data signal of the bus signal [ "*Configure segment screen presentation may further include power supply input portion 606 via which a user provides the tool 120 with the voltage of the power supply that is used by the segment of the process control network.*" (column 6, lines 50-53)].

Regarding claim 7, Stewart discloses that the bus signal has a structure that is the same at an output port of the operation block as at an input port of the operation block [ "*The bus 102 also may include one or more junction boxes 104 (JB1, JB2, JB3), which are often referred to as*

"bricks." (column 4, lines 10-15); FIG. 8A showing the Fieldbus connector entering from the left (FFI) and leaving to the right (H1)].

Regarding claims 10 and 37, Stewart discloses validating a constraint on the bus signal [*"The method includes a software analysis tool having access to information regarding standard protocol criteria including a length of the bus, a cable type of the bus and a voltage requirement of the field device for analysis by the tool to assure that the process control network design conforms to the criteria of the standard protocol."* (column 2, lines 49-58)].

6. Claims 1-7, 9-10, 32-37, and 42 are rejected under 35 U.S.C. § 102(b) as being anticipated by US Patent No. 6,470,482 to Rostoker et al. (Rostoker).

Regarding claim 1, Rostoker discloses a method comprising the steps of:

Grouping a first data signal of a first signal type and a second data signal of a second signal type to form a bus signal in a graphical model displayed on a graphical user interface [*"A bus signal line 2220 (CTRL<0...3>, representing four physical "wires") connects between the graphical representation 2216 of the microprocessor 2116 and the graphical representation 2214 of the controller 2114 and extends off towards the right hand side of the display screen 2200 (as depicted)." (column 32, lines 46-51)]; and*

Performing a non-virtual operation on the bus signal [the bus 2220 connects to graphical representation 2214 of the controller 2114, and *"The design description 2114a for the other*

*controller 2114 (CHIP 3) refers to a core cell 2128 (CORE 'C') and a logic block 2130 (misc. logic 'C')."* (column 32, lines 31-33)].

Regarding claim 2, Rostoker discloses that the graphical model is a block diagram (FIG. 22), and the step of performing a non-virtual operation on the bus signal comprises constructing the block diagram including an operation block representing the non-virtual operation (ref. 2214, FIG. 22) and connecting a representation of the bus signal in the block diagram to an input port of the operation block (ref. 2220 is connected to ref. 2214, FIG. 22).

Regarding claim 3, Rostoker discloses that an outlet of the operation block connects to a modified bus signal comprising a modified first data signal, where the modified first data signal represents an output of the non-virtual operation where the first data signal is an input to the non-virtual operation, and a modified second data signal, where the modified second data signal represents an output of the non-virtual operation where the first data signal is an input to the non-virtual operation [FIG. 22, where input bus "CTRL<0..3>" ref. 2220 connects to operation block ref. 2214, which in turn is connected to output bus "C<0..3>".].

Regarding claim 4, Rostoker discloses that the step of performing a non-virtual operation represented by the operation block comprises solving the non-virtual operation using values represented by the first data signal and the second data signal as inputs to the non-virtual operation [*"A microprocessor 2116 (CHIP 1), two controller chips 2110 and 2114 (CHIP 2 and CHIP 3, respectively) and nine memory chips 2112 (CHIP 4) are included in the design."*

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(column 32, lines 12-18); *"The design description 2114a for the other controller 2114 (CHIP 3) refers to a core cell 2128 (CORE "C") and a logic block 2130 (misc. logic "C")."* (column 32, lines 31-34); *"A bus signal line 220 (CTRL<0...3>, representing four physical "wire") connects between the graphical representation 2216 of the microprocessor 2116 and the graphical representation 2214 of the controller 2114..."* (column 32, lines 46-51)]. Rostoker discloses that block 2214 corresponds to a memory controller 2114, receiving input bus "CTRL<0..3>", operating on the same to perform memory controller functions, and producing the output bus "C<0..3>", as disclosed by FIGS. 21-22.

Regarding claim 5, Rostoker discloses converting the graphical model to executable computer readable instructions representing the graphical model and executing the computer readable instructions, wherein the computer readable instructions implement the functionality specified by the model [*"The logic compiler takes the net list as an input, and using the component database puts all of the information necessary for layout, verification and simulation into a schematic object file or files whose format(s) is(are) optimized specifically for those functions. The logic verifier checks the schematic for design errors, such as multiple outputs connected together, overloaded signal paths, etc., and generates error indications if any such design problems exist. The logic simulator takes the schematic object file(s) and simulation models, and generates a set of simulation results, acting on instructions initial conditions and input signal values provided to it either in the form of a file or user input."* (column 9, lines 1-15)].

Regarding claim 6, Rostoker disclose the step of defining one or more physical attributes for the first data signal and the second data signal of the bus signal [FIG. 22, ref 2200. The first signal 0 is physically connected to blocks 2216 and 2214. The second signal 1 is physically connected to blocks 2216 and 2214.].

Regarding claim 7, Rostoker discloses that the bus signal has a structure that is the same at an output port of the operation block as at an input port of the operation block [FIG. 2, input bus "CTRL<0..3>" has the same structure as output bus "C<0..3>." Both input and output bus comprise four physical "wires."].

Regarding claim 9, Rostoker discloses that the first signal type and the second signal type are different [FIG. 22, ref 2200a depicts first signal 0 at a logic "high" during the third interval, while second signal 1 is at a logic "low" during the third interval. Thus the first and second signal have a different type during the second interval.].

Regarding claim 10, Rostoker discloses validating a constraint on the bus signal [*"The logic synthesis process 2304 provides indications on information about design rule violations 2308. This information includes data about what signals and components of the design are in violation of the rules. In response, the schematic display system calls up an appropriate schematic diagram (i.e., a schematic diagram on which the offending signal, signals, and/or components can be found) and displays the schematic diagram and simulation results corresponding to the design rule violations 2308."* (column 33, lines 44-59)].

Claims 32-37 recite a medium holding computer-executable instructions for performing the method of claims 1, 2, 4, 5, 6, and 10. As Rostoker discloses a computer-implemented method (FIG. 8), Rostoker anticipates claims 32-37 for the reasons set forth above regarding claims 1, 2, 4, 5, 6, and 10.

Regarding claim 42, Rostoker discloses a system for generating and displaying a modeling application for simulating a dynamic system, comprising:

A user-operable input means for inputting data to the application [(FIG. 8, “Graphical User Interface 806”); *“A pointing device is any device through the use of which a user may ‘point’ to and identify objects on a display screen...”* (column 3, lines 33-45, etc.)];

A display device for displaying a graphical model representing the dynamic system (FIG. 8, “Graphical User Interface 806”); and

An electronic device including memory for storing computer program instructions and data, and a processor for executing the stored computer program instructions (column 1, line 25 – column 2, line 4), the computer program instructions including instructions for performing a non-virtual operation on a bus signal displayed in a graphical model (FIG. 22, ref 2216, 2220, 2214), wherein the bus signal comprises a first data signal of a first signal type and a second data signal of a second signal type grouped together to form the bus signal [(FIG. 22, ref 2200, 2200a), first signal 0 of first signal type “high” during the third interval, second signal 1 of a second type “low” during the third interval].

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. § 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. § 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. § 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. § 103(c) and potential 35 U.S.C. § 102(e), (f) or (g) prior art under 35 U.S.C. § 103(a).

7. Claim 8 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Rostoker as applied to claim 2 in view of "SIMULINK Model-Based and System-Based Design Version 4" by The MATHWORKS (Simulink).

Regarding claim 8, Rostoker does not expressly teach that the non-virtual operation comprises one of the claimed operations.

Simulink teaches a dead zone function (page 9-66).

Rostoker and Simulink are analogous prior art because both are directed to simulation.

It would have been obvious to a person of ordinary skill in the art at the time of Applicants' invention to combine the teachings of Rostoker and Simulink because Simulink provides a graphical user interface which enhances usability and does not require a user to formulate complicated equations [ "*For modeling, Simulink provides a graphical user interface (GUI) for building models as block diagrams, using click-and-drag mouse operations. With this interface, you can draw the models just as you would with pencil and paper (or as most textbooks depict them). This is a far cry from previous simulation packages that require you to formulate differential equations and difference equations in a language or program. Simulink includes a comprehensive library of sinks, sources, linear and nonlinear components, and connectors.*" (Simulink, pages 1-2 to 1-3)].

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of Applicants' invention to combine the teachings of Rostoker and Simulink by using a dead zone function in the controller 2114 to arrive at the claimed invention.



*Conclusion*

Art considered pertinent by the examiner but not applied has been cited on form PTO-892.

US Patent No. 6,883,147 discloses a method and system for simulation of bus circuits and bus interfaces to logic blocks (abstract, FIG. 4B).

US Patent No. 6,163,763 discloses a method of bus functional modeling (FIG. 3, etc.) which teaches aspects of the presently claimed invention but does not teach the disclosed invention (for example, present application, Fig. 5).

“SmartVehicle Challenge Problems” by William Milam and Alongkrit Chutinan appears to teach a prior art method of bus implementation in a graphical user interface (Figure 5, page 8).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jason Proctor whose telephone number is (571) 272-3713. The examiner can normally be reached on 8:30 am-4:30 pm M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Paul Rodriguez can be reached at (571) 272-3753. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.


Any inquiry of a general nature or relating to the status of this application should be directed to the TC 2100 Group receptionist: 571-272-2100. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR)

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system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jason Proctor  
Examiner  
Art Unit 2123

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